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Attorney Docket No.: 291958170US2  
Semitool Ref. No.: P99-0006US3  
(PATENT)

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Patent Application of:  
Ritzdorf et al.

Application No.: 09/885,451

Confirmation No.: 3390

Filed: June 20, 2001

Art Unit: 1742

For: METHOD AND APPARATUS FOR LOW  
TEMPERATURE ANNEALING OF  
METALLIZATION MICRO-STRUCTURES IN  
THE PRODUCTION OF A  
MICROELECTRONIC DEVICE

Examiner: W. T. Leader

**DECLARATION OF THOMAS L. RITZDORF UNDER 37 C.F.R. § 1.131**

MS Amendment  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

I, Thomas L. Ritzdorf, declare and state that:

1. I am a joint inventor, along with LinLin Chen, Henry Stevens, Lyndon W. Graham, and Curt Dundas, of the invention described and claimed in U.S. Patent Application No. 09/885,451 filed on June 20, 2001, which is a continuation of U.S. Application No. 09/387,577 filed on August 31, 1999 (now U.S. Patent No. 6,508,920), which is a continuation of International Application No. PCT/US99/02504, designating the United States, filed February 4, 1999, which is a continuation-in-part of U.S. Application No. 09/018,783, filed February 4, 1998, and claims the benefit of U.S. Provisional Application No. 60/087,432, filed June 6, 1998. This declaration establishes that the

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invention was made in this country before February 3, 1998, and thus before the U.S. filing date of U.S. Application No. 09/017,676 issued to Dubin (now U.S. Patent No. 6,249,055).

2. Before February 3, 1998, the above-listed joint inventors and I conceived the invention presented in the above-captioned patent application as corroborated by (a) the redacted paper entitled "*On The Self-Annealing Of Electrochemically Deposited Copper Films*" (hereafter the "Annealing Paper" and attached hereto as Exhibit A), and (b) the redacted Process of Record Document referenced in the Annealing Paper with respect to depositing metal onto workpieces (herein the "POR Document" and attached hereto as Exhibit B). Both the Annealing Paper and the POR Document were completed before February 3, 1998, and the work discussed in the Annealing Paper was also completed before February 3, 1998.

3. As indicated in the Annealing Paper, the above-listed joint inventors and I conceived of a process in which a workpiece is exposed to an electrolytic solution containing metal ions to deposit the metal onto the workpiece. (Annealing Paper at ¶ 1, and POR Document at § 4.) We conceived of depositing metal onto the workpiece by applying plating power at a first current density for a first period of time to deposit a first amount of metal onto the workpiece, and subsequently applying a second current density for a second period of time to deposit a second amount of metal onto the first amount of metal. The second current density is greater than the first current density such that a majority of the metal is deposited onto the workpiece using the second current density. (Annealing Paper at ¶ 3, and POR Document at § 4.) We also conceived of subjecting the surface of the workpiece to an elevated temperature annealing process after depositing the metal using the first and second current densities. (Annealing Paper at ¶ 9 and Figure 5.)

4. I, along with the above-listed joint inventors, also invented the features covered in the dependent claims. More specifically, we invented performing the foregoing process on a workpiece surface having recessed microstructures less than 0.5 microns wide, such as 0.3 microns (POR Document at § 5-"Gap Fill Capability"), and we conceived

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of applying the second current density immediately after the first current density (POR Document at § 4-"Electroplating Process Recipe for 1.5  $\mu\text{m}$  Cu"). We further invented using particular current densities (POR Document at § 4-"Power Supply Set Points"), limiting the duration of applying the first current density to 30 seconds (POR Document at § 4-"Electroplating Process Recipe for 1.5  $\mu\text{m}$  Cu"), and annealing the deposited copper at an elevated temperature (Annealing Paper at ¶ 9).

5. The general practice at Semitool, Inc. (the assignee of this invention) is to establish a Process of Record only after sufficient analysis and development have been completed for a particular process to enable the use of the process on customer products. Accordingly, the Process of Record documents a particular process and the equipment on which the process is carried out, and the completion of a Process of Record is an indication that the process has been successfully carried out and characterized using actual hardware. The POR Document was developed according to the general practice at Semitool, Inc.

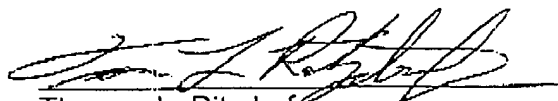
6. As established by the Annealing Paper and the POR Document, we reduced the invention to practice before the February 3, 1998, effective date of U.S. Patent No. 6,249,055.

7. I further declare that all statements herein made of my own knowledge are true, and that all statements made on information or belief are believed to be true; and further, that the statements are made with the knowledge that the making of willful or false statements or the like is punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and may jeopardize the validity of any patent issuing from this patent application.

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Dated this 18<sup>th</sup> day of March, 2005.

  
Thomas L. Ritzdorf

Residence : 3130 Parkwood Lane  
Big Fork, MT 59911

Citizenship : United States

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**EXHIBIT A**

## On the Self-Annealing of Electrochemically Deposited Copper Films

### Introduction

Electrochemical deposition, or ECD, of copper films has become an important process step in the manufacturing of high performance semiconductor products. ECD is being used to deposit copper on the surface of semiconductor wafers for the purpose of filling submicron trenches and vias for multilevel metal interconnection. Copper has obvious advantages in terms of the material specific resistivity, which translates into faster processing speeds. Copper also has a theoretical advantage in terms of electromigration resistance, although this is realized to different extents, depending on the processing conditions used. One factor that has a very large influence on the electromigration resistance of submicron metal lines is the grain size. This is due to the fact that grain boundary migration occurs with a much lower activation energy than intra-grain migration.

The phenomenon of self-annealing, or annealing at room temperature, that is seen in some ECD copper films can be used advantageously to produce a desired grain structure that results in reliable interconnect lines. This property can be used to separate the process variables that lead to the best trench fill results from those that lead to long-term reliability. In other words, process conditions that lead to optimum filling of submicron features can be used, if they also promote the self-annealing of the deposited film in such a way as to promote device reliability.

### Experimental

Several copper films were prepared on silicon wafers using electrochemical deposition. All samples used for this study were blanket films of 1.5  $\mu\text{m}$  thickness. The substrate wafers were 200 mm silicon wafers with approximately 1.0  $\mu\text{m}$  of silicon dioxide deposited on the silicon. A barrier layer of 500 Å to 1000 Å of TaN, and a seedlayer of 1000 Å of copper were deposited on the oxide, to provide a base conductive layer for the electrochemical deposition. All samples had 1.5  $\mu\text{m}$  of copper deposited on this structure using a Semitool single wafer ECD chamber. The process used for this deposition was the Semitool process of record (CuPOR97.09), which consists of a low current initiation step, followed by a square-wave current pulse waveform for the bulk of the deposition. Subsequent to the deposition, the wafers used for this experiment were subjected to various time and temperature treatments, as indicated below, and several measurements of the material properties were made.

One experiment involved simply allowing several wafers to remain at ambient temperature (approximately 25°C) over a period of several weeks, while several measurements were made at intervals over this time. Measurements included sheet resistance, stress, and X-ray diffraction analysis.

Another experiment was performed to make an estimate of the activation energy of the material change that caused variations in the measured parameters. In this experiment, several wafers were prepared, as above, and subjected to different temperature treatments. The sheet resistance was measured at intervals over time and the variations in time required to undergo a change in sheet resistance of half the total change was recorded. Since these films typically undergo a reduction in sheet resistance of approximately 20%, the time required for the sheet resistance to decrease by approximately 10% was recorded. These times and temperatures were used to calculate the activation energy of the process which results in the decrease of sheet resistance.

## Results and Discussion

Wafers held at room temperature for extended periods of time after having a copper film deposited by ECD have been shown to undergo a change in sheet resistance over a period of several days. Presently, this change is believed to be due to a stress/strain relaxation which leads to a reduction of dislocation density, or to growth of the copper grains themselves. Several wafers had copper deposited to a nominal thickness of 1.5  $\mu\text{m}$ , and were subjected to measurements of several properties over time. One wafer was held at Semitool and its sheet resistance was measured as a function of time. The results of this measurement were very similar to previous measurements, as seen in the graph in figure 1. It is also interesting to note that the within wafer uniformity, or sheet resistance standard deviation, increases for a period of time (while the slope of the sheet resistance vs. time plot is high) before returning to near its original value. This result can be seen in figure 2.

Three additional wafers were sent to Intel, in Santa Clara, California, for measurements of sheet resistance, copper film stress, and X-ray Diffraction measurements (XRD). These results tell a similar story. The sheet resistance exhibited a behavior similar to that seen in Kalispell, with a similar time dependence. The temperature-adjusted film stress measured on a Tencor Flexus system started at approximately 13 MPa and increased over a period of approximately 25 hours to about 18 MPa. This timeframe also correlates well to the sheet resistance changes, although the fact that the film stress is increasing is not exactly what was expected.

The XRD measurements show a fairly dramatic increase in the texture, or orientation, of the film over time. The ratio of intensity of the (111) peak area to the (200) peak increased dramatically within approximately 8 hours after deposition, and at the same time the peak widths of both peaks decreased. The decrease in peak widths indicates better alignment of the grains, while the increased intensity ratio (from 118 to over 1400) indicates that a much larger proportion of the volume has become oriented with a (111) texture normal to the surface plane. This effect is also seen in the fact that the area of the rocking curve peak is seen to increase from 61545 to 196238 over the same period of time, while also becoming sharper.

The second experiment consisted of holding wafers at different temperatures and measuring changes in sheet resistance over time. The time at which the change in sheet resistance was half complete was used to calculate an activation energy for the process that induces the change in sheet resistance of the sample. This sheet resistance was calculated to be approximately 1.1 eV for data taken at 2°C, 25°C, and 62°C. The sheet resistance versus time plots of these samples are seen in figure 5, and the Arrhenius plot, which was used to calculate the activation energy is seen in figure 6.

## Consequences

These data indicate that the grain size of electrochemically deposited copper is growing (and becoming more oriented) significantly subsequent to the deposition process. This grain growth is useful in that it serves to produce the large grains that are desirable from the point of view of electromigration resistance, while allowing the deposition conditions to be such that small grains are produced, which is normally what is desired for optimal trench and via fill performance. This is a very useful property, in that it can serve to decouple the process conditions that are necessary for filling from those that produce desirable electrical results. This allows the process engineer to design the process in a way that produces small grains and optimal filling, while controlling the self-annealing property to subsequently provide the large (bamboo structure) grains that are desirable from an electrical performance standpoint.

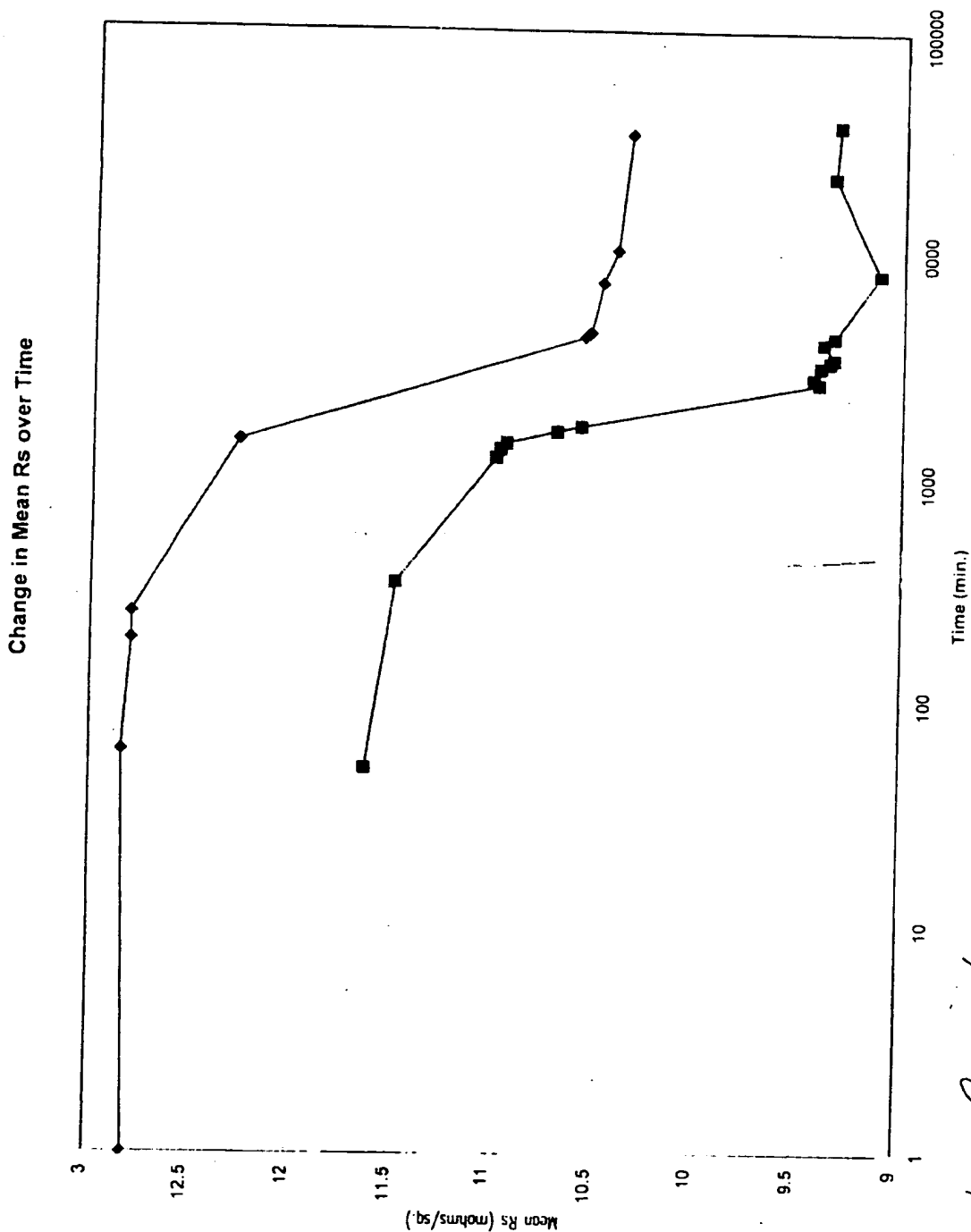
## References

1. Microstructural stability of Copper Electroplate; B.M. Hogan; Los Alamos Scientific Laboratory; AES Conference.
2. The Influence of Pulse Frequency on the Hardness of Bright Copper Electrodeposits; D.S. Stoychev, M.S. Aroyo; Plating and Surface Finishing; August 1997; pp. 26-28.
3. Recovery and Recrystallization of Electrodeposited Bright Copper Coatings at Room Temperature. II. X-Ray Investigation of Primary Recrystallization; I.V. Tomov, D.S. Stoychev, I.B. Vitanova; Journal of Applied Electrochemistry 15(1985); pp887-894.
4. The Self-Annealing of Copper; M. Cook, T.L. Richards; J. Inst. Met. 70(1944); pp 159-173.





Sheet1 Chart 1



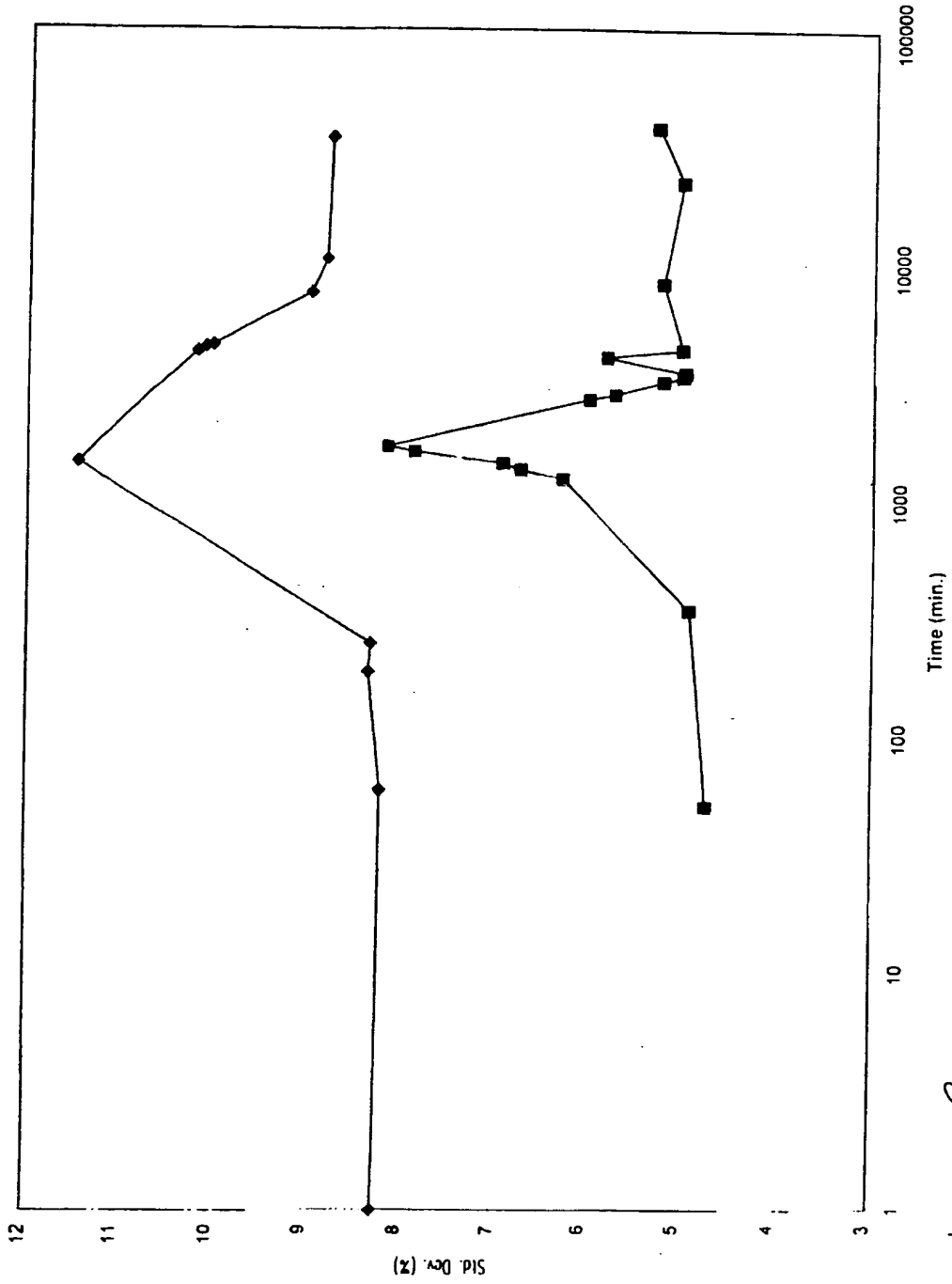
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Figure



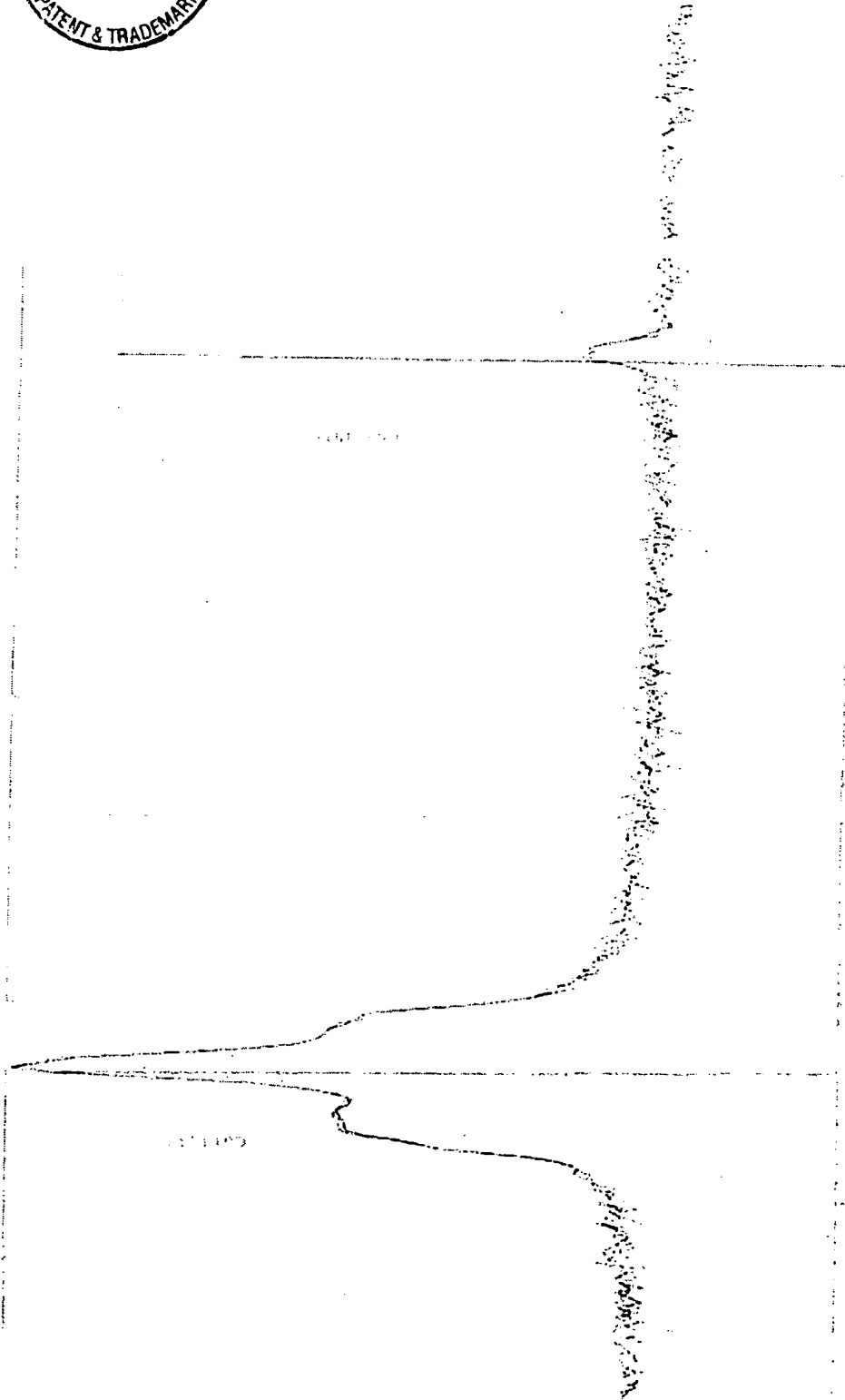
Sheet1 Chart 2

Change in Standard Deviation over Time



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Figure 2.

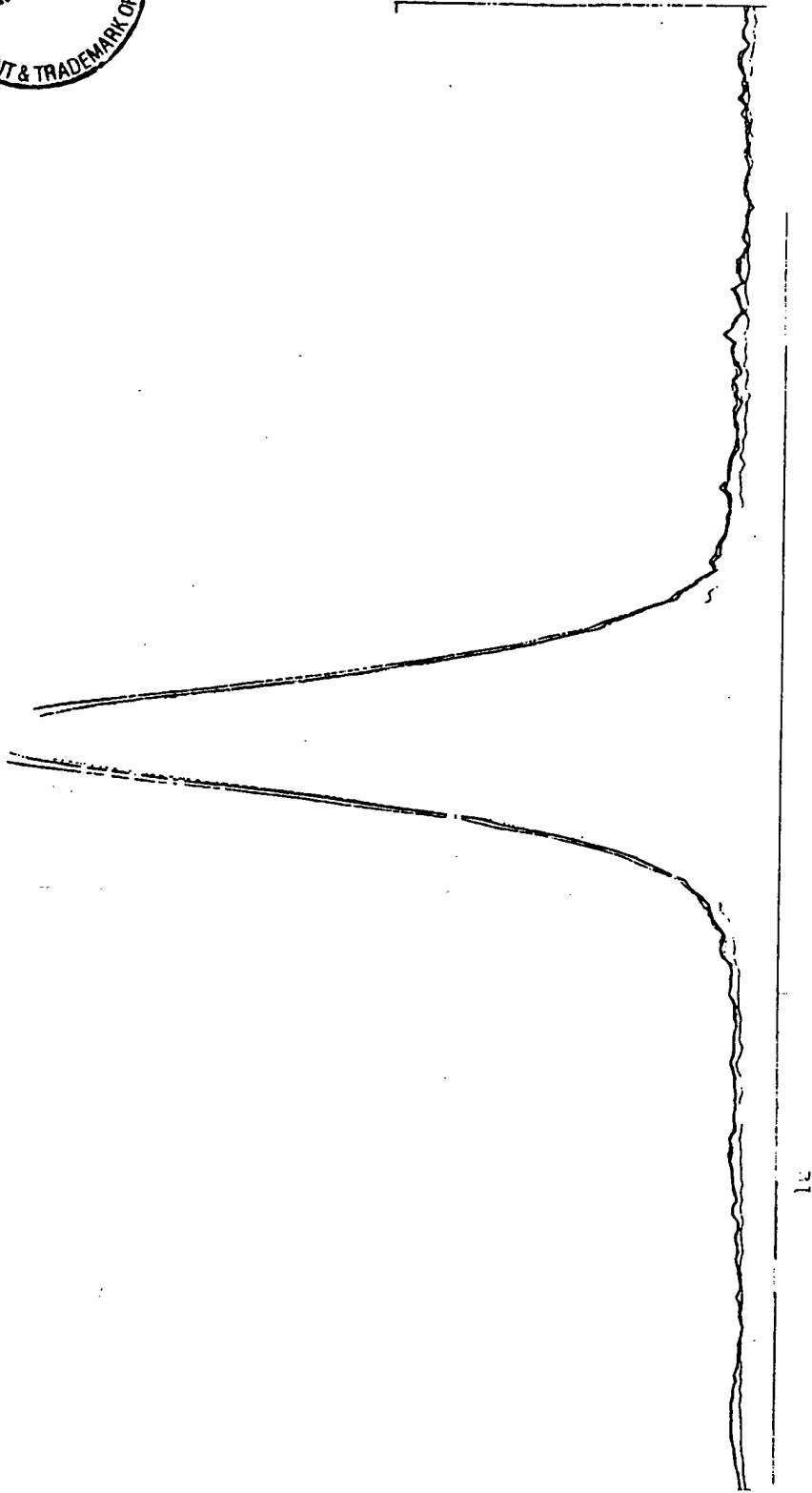


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See also Appendix A

Fig. 3a

Figure 3



Submitted: *Dr. P. K. Singh*  
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Figure 4



Sheet1 Chart 2

Sheet Resistance vs. Time

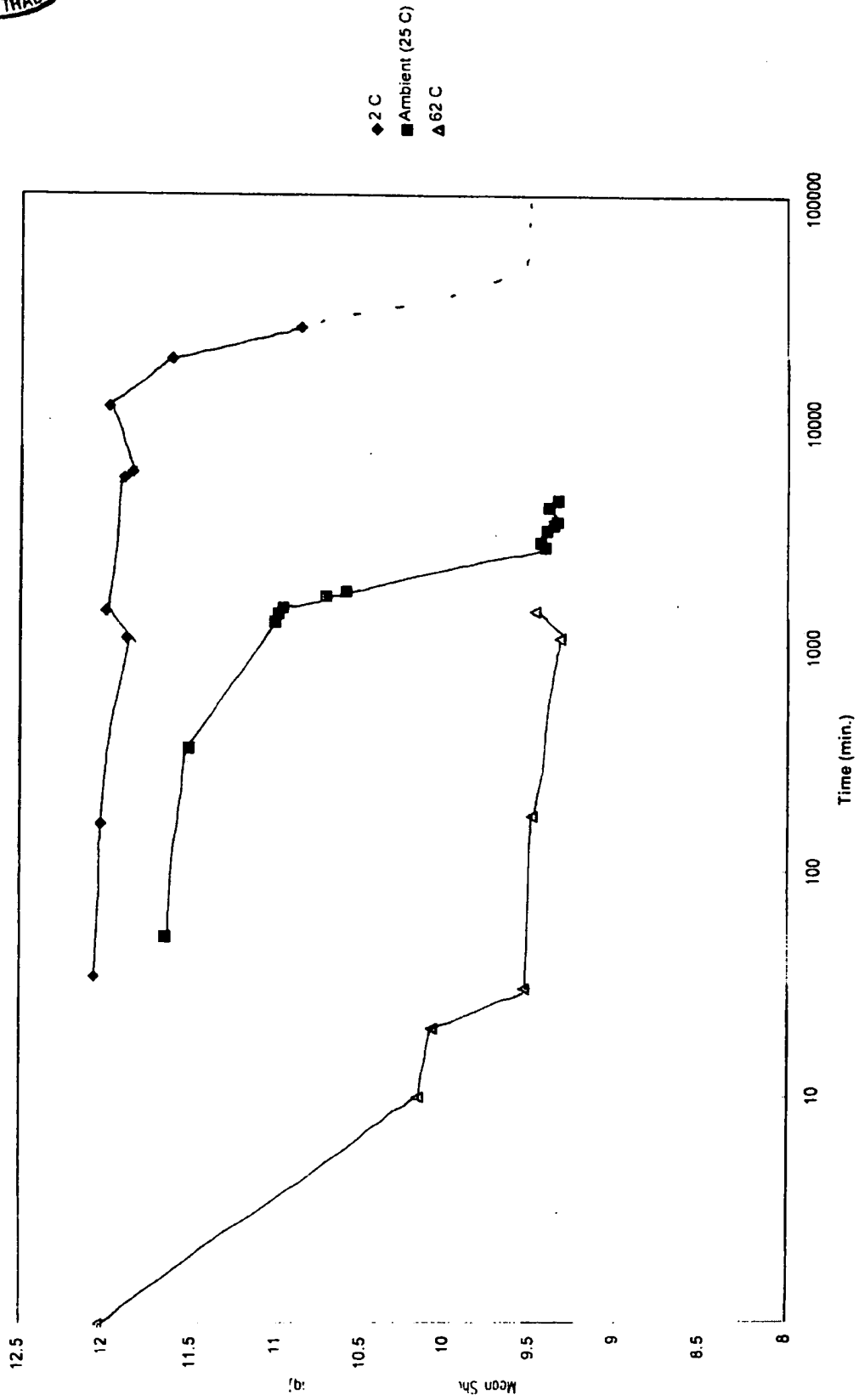


Figure 5

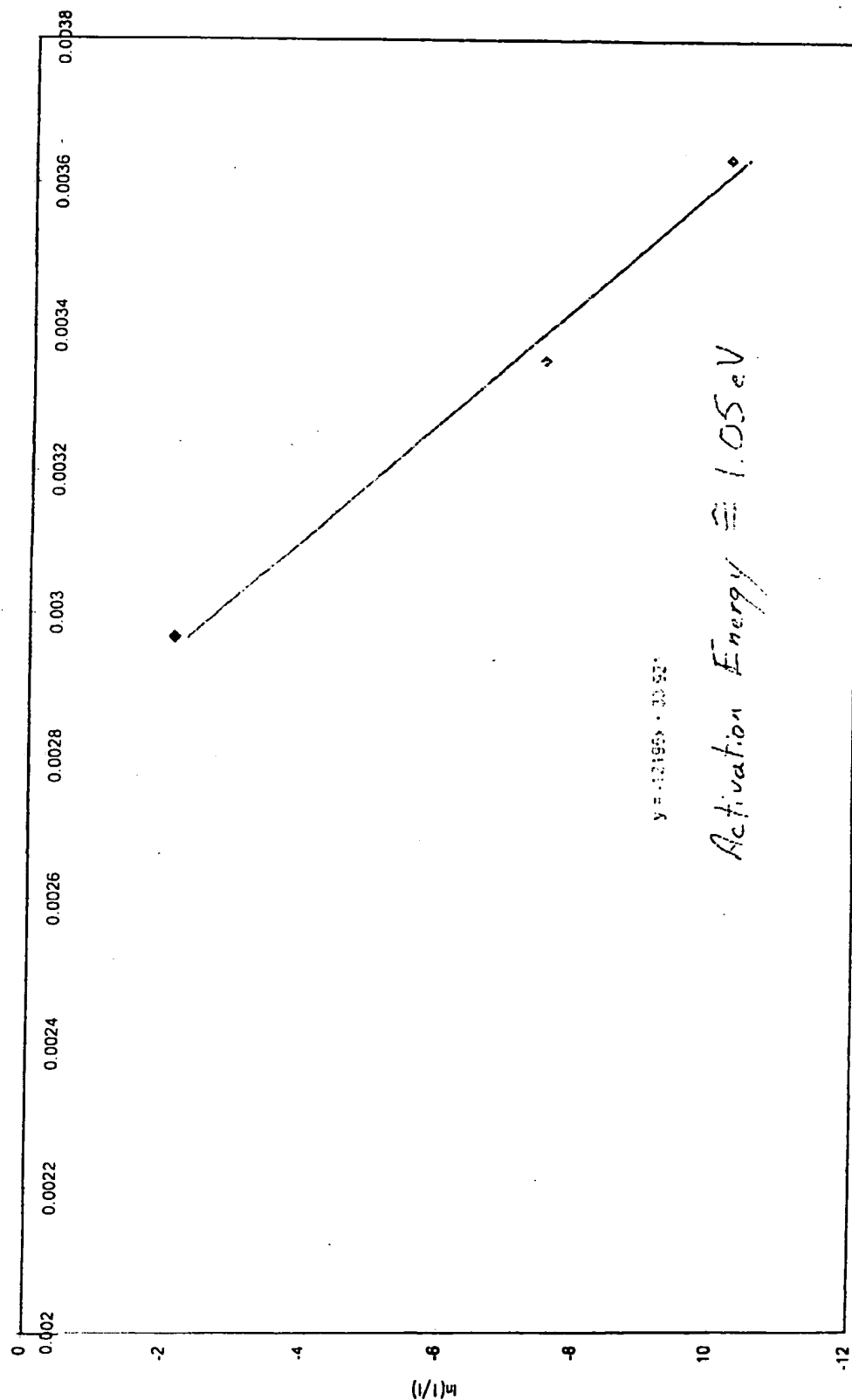
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Sheet1 Chart 1

Arrhenius Plot for Self-Annealing



1/T (K<sup>-1</sup>)

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Figure 6

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**EXHIBIT B**

# SEMITOOL®

## Advanced Technology Process Group

655 West Reserve Drive, PO Box 7010, Kalispell, MT 59904 Phone: 406-752-2107 Fax: 406-752-5522

To: Bob Berner

From: Jeff Turner

Subject: POR Document - Rev. [REDACTED]

cc: Ed Fix, Blaine Wright, Tom Oberlitner, Thomas Taylor

---

### 1) Objective of POR Change

Improving uniformity

### 2) Changes from Rev. 1.1:

Part #'s for appropriate fingers, diffusers, and rotors

Process Performance Capabilities - uniformity

Low Current Initiation

Finger Season Recipe

Power Supply Capability

Bowl assy #, diffuser to be called by process engineering

### 3) Hardware Requirements

- POR Hardware assembly #'s for 200 mm Consumable Cu Plating

Assembly #	Assembly Description
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100T0041	200mm consumable plating bowl assembly
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LT01200	Drive head assembly
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LT01225	Rotor assy J-hook, 60° cam 1 mm edge excl
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LT01210	Rotor assy J-hook, 90° cam 2.5 mm edge excl
---------	---

\*all assembly drawings attached

*Note: Assembly drawings 100T0041 and LT01225 or LT01210 need to have the finger and diffuser numbers changed to the corresponding numbers depending on the customers requirements*

#### Additional Hardware Requirements

##### Diffusers

1mm edge exclusion	111T0146
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2.5 mm edge exclusion	111T0147
-----------------------	----------

*Note: Diffusers to be specifically called out in the process spec sheet filled out by the process engineering group.*

##### Fingers

Partially coated J-hook	213T0073
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- Power Supply Requirements      attachment: power supply sheet

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One 10/20/60 channel per ECD module

- Chamber Configuration
  - Top of Diffuser to top of Upper Cup 2.0 cm
  - Top of Diffuser to top of Anode 1.6 cm

#### 4) Process Requirements/Parameters

##### Chemistry

- Electrolyte - "Enthone-OMI Cu Bath M Make-Up Solution"

Composition	CuSO <sub>4</sub> *5H <sub>2</sub> O	67 g/l (Cu 17 g/l)
	H <sub>2</sub> SO <sub>4</sub>	170 g/l
	HCl	70 ppm
- Additive Solutions
  - Enthone-OMI Cu Bath M - D 6.4 ml/l (make-up)
  - Enthone-OMI Cu Bath M LO 70/30 Special 1.6 ml/l (make-up)
- Additive Replenishment Algorithm at 5.5 GPM Flowrate
  - MD  $Add = C_i - C_o - (A) + ((0.206(t)(C_p) + 0.0288(Ch))/V)$
  - LO 70/30 Special  $Add = C_i - C_o - (A) + ((0.014(Ch))/V)$

##### Legend

Add	Amount of MD or LO 70/30 Special to add in <i>ml/l</i>
C <sub>i</sub>	Ideal MD bath concentration in <i>ml/l</i>
C <sub>o</sub>	Last known concentration of MD or LO 70/30 Special in <i>ml/l</i>
A	Amount of MD or LO 70/30 Special added since last known concentration in <i>ml/l</i>
t	Elapsed time since last known concentration in <i>min</i>
Ch	Charge transferred since last known concentration in <i>Amp*min</i>
V	Total plating bath volume in <i>Liters</i>
C <sub>p</sub>	# of process chambers on line

##### Process Recipes

- Electroplating Process Recipe for 1.5 µm Cu

Step	Description	Time
1	Dwell (pre-plate)	0:05
2	Low I initiation	0:30
3	ECD	3:40
4	Lift to crack pos.	0:02
5	Spin-off @ 500 rpm	0:05
Total Recipe Time		4:22

- Plating cell parameters
  - Flow Rate 5.5 gpm
  - Temperature 25 °C
  - Rotation for ECD 20 rpm

Power Supply Setpoints (forward only waveform)

Step 1 (low I initiation)

I<sub>r</sub> 1.0 Amps (200 mm wafers) - 0.5 amp\*min  
0.6 Amps (150 mm wafers) - 0.3 amp\*min

Step 2 (ECD step)

I<sub>r</sub> 8.6 Amps (200 mm wafers) - 23.4 amp\*min  
4.9 Amps (150 mm wafers) - 13.1 amp\*min

Nominal Thickness - 1.5  $\mu$ m

Timing	Fwd on	95 ms
	Fwd off	35 ms
	Fwd Total	130 ms
Peak Cathodic Current Density		28 mA/cm <sup>2</sup>

- Finger Seasoning Recipe

0.4 Volts, DC for 3:00

*Note: fingers must be in the open position*

- Contact In-Situ Clean  
NA

- Spin-Rinse Dry Recipe

Step	Description	Time	RPM
1	Rinse M1, M3	0:15	50
2	Rinse M1, M3	0:15	300
3	Rinse M3	0:15	50
4	Dry N <sub>2</sub> M2	0:30	1800
5	Dry N <sub>2</sub> M2	1:00	600

Total Recipe Time 2:15

- Pre-Wet Recipe (Optional)

Step	Description	Time	RPM
1	T1 to M1 to T1	0:20	50
2	N <sub>2</sub> to M1 to T1	0:02	50
3	Rinse M1, M3	0:08	50
4	Rinse M1, M3	0:07	300
5	Rinse M3, asp M1	0:05	50
6	Dry N <sub>2</sub> M2	0:30	1800
7	Dry N <sub>2</sub> M2	0:30	600

Total Recipe Time 1:42

## 5) Process Results

Plating Rate		3600 Å/min average
Plating Uniformity	cross wafer	3 sigma, +/- 10 % average
	wafer to wafer	3 sigma, +/- 10 % average
Gap Fill Capability		Void free fill at $\geq 0.3 \mu\text{m}$ , $\leq 1.2 \mu\text{m}$ depth 4:1 AR
Cu Film Specific Resistivity		$\leq 2.1$ micro ohm cm
Grain Size		Mean diameter on planar wafers $\geq 0.5 \mu\text{m}$
Film Impurities		$\leq 150$ ppm total (C, Cl, Fe, S, P, ...)
Wafer Contact Life*		$\geq 200$ hours at maximum throughput
Electrolyte Bath Life		30 wafers/liter (720 Amp*min/liter)
	*1.5 $\mu\text{m}$ nominal thickness on 200 mm wafers	